

Customer No.: 31561
Application No.: 10/063,576
Docket No.: 8317-US-PA

REMARKS

Present Status of the Application

The Office Action dated August 10, 2004, objected drawings for not showing every feature if the invention specified in the claims. Claims 10-18 and 20-31 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Claims 1-5, 10-14, 17-18, 22-27 and 30-31 were rejected under 35 U. S. C. 103(a) as being unpatentable over Akram (US Patent 5,903,058) in view of Charkraworty and Kimijima et al. (JP 08-213399). Claims 6, 8-9, 15-16, 20-21 and 28-29 were rejected under 35 U. S. C. 103(a) as being unpatentable over over Akram in view of Charkraworty and Kimijima et al., and further in view of Hosaka (U.S. Patent 6,475,897).

Applicants have amended claim 10 for deleting the feature not shown in the figures. After entry of the amendments and considering the following remarks, reconsideration and withdrawal of these rejections are respectfully requested.

Discussions of the objections for drawings

Drawings were objected for not showing every feature if the invention specified in the claims, especially a redistribution layer on the active surface of the wafer or an under ball metallurgy (UBM) on a redistribution layer.

Claim 10 has been amended by canceling these features not shown in the figures.

Withdrawal of these objections is respectfully requested.

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Discussion of the 112 rejections

Claims 10-18 and 20-31 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The Office Action considered “forming an UBM on a redistribution layer on the active surface of the wafer” in claim 10 and “bonding a plurality of conductive studs onto the UBM by wiring bonding, wherein each conductive stud has a top surface and a bottom surface opposite to the top surface, wherein the bottom surface is in contact with the UBM and the top surface is flattened by polishing for coplanarity after the conductive stud is bonded onto the UBM; and partially removing the UBM using the above conductive studs as masks until the active surface of the wafer is exposed” in claim 22 are not supported by the specification and figures.

Claim 10 has been amended by canceling the redistribution layer.

However, for the feature specified in claim 22, the supporting ground can be found in paragraph [0033] of the specification and Figure 16.

Reconsideration and withdrawal of these rejections are respectfully requested.

Discussions of the 103 rejections

Claims 1-5, 10-14, 17-18, 22-27 and 30-31 were rejected under 35 U. S. C. 103(a) as being unpatentable over Akram (US Patent 5,903,058) in view of Charkraworty and Kimijima

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et al. (JP 08-213399). Claims 6, 8-9, 15-16, 20-21 and 28-29 were rejected under 35 U. S. C. 103(a) as being unpatentable over over Akram in view of Charkraworty and Kimijima et al., and further in view of Hosaka (U.S. Patent 6,475,897).

Applicants respectfully traverse the rejections for at least the reasons set forth below.

As stated by the Office Action, Akram failed to teach the requisite steps of bonding a conductive stud "by wiring bonding" and "the top surface of the conductive stud is flattened by polishing so that the top surfaces of the conductive studs are coplanar". The Office Action considered that Akram substantially discloses the claimed method, and relied on Charkraworty for teaching using wire bonding and Kimijima for teaching flattening the conductive stud.

Even if considering wire bonding as equivalent technique to stenciling as asserted by the Office Action, no motivation is equitably provided for one skilled in the art to modify Akram's method by using both teachings from Charkraworty and Kimijima.

Although Charkraworty discloses using wire bonding as one possible method of depositing the metal bumps 311-1, nothing is mentioned or suggested by Charkraworty in relating to the purposes and advantages of using wire bonding. Moreover, Charkraworty fails to recognize the values of flattening the top surface of the formed conductive studs for coplanarity and Charkraworty conversely teaches polishing the conductive studs after encapsulation to expose the stud for external connection. On the other hand, Kimijima teaches forming solders 20 by plating, and as emphasized by Kimijima, the polishing

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process is performed to the solder in order to solve the problems caused by the plating process (see [problems to be solved by the invention]).

Therefore, even if one skilled in the art considers modifying Akram's method with Charkraworty's teachings of bonding the conductive studs by wire bonding, because wire bonding is adopted for forming the conductive studs and there is no such concern of solders having different sizes due to the plating process, one skilled in the art will not contemplate to flatten the top surface of the stud by polishing. Obviously, the combined teachings of the references do not suggest one skilled in the art to incorporate Kimijima's polishing process for solving the problems arisen from using plating, into Akram's method modified with Charkraworty's wire bonding technique.

Hosaka merely discloses certain materials for bumps, but does not suggest the combination of features recited in dependent claims. Therefore, Hosaka fails to remedy the deficiencies of the above cited references.

Furthermore, none of the cited references recognize the advantages of this invention. According to the present invention, the composition and volume of the conductive studs can be controlled more precisely by using wire bonding and flattening top surfaces of the conductive studs by polishing, which greatly enhances bumping strength.

Accordingly, Applicants respectfully submits that independent claims 1, 10 and 22 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims patently define over the prior art references as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date :

Nov. 10, 2004

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